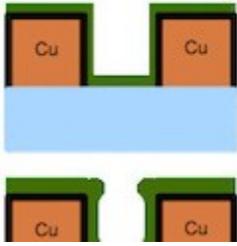


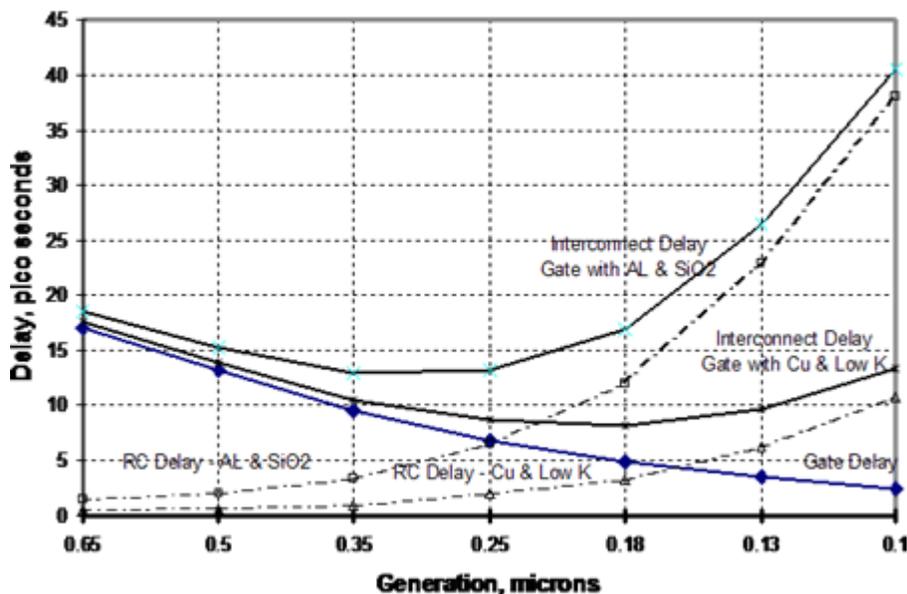
Air-gaps in Copper Interconnects for Logic



By Ed Korczynski, Sr. Technical Editor, SST/SemiMD

The good people at ChipWorks have released some of the first public data on [Intel's new 14nm-node process](#), and the results indicate that materials limitations in on-chip electrical interconnects are adding costs. Additional levels of metal have been added, and complex "air-gap" structures have been added to the dielectric stack. Flash memory chips have already used air-gaps, and IBM has already used a subtractive variant of air-gaps with >10 levels of metal for microprocessor manufacturing, but this is the first known use of additive air-gaps for logic after Intel announced that a fully-integrated process was ready for 22nm-node chips.

Mark Bohr of Intel famously published data in 1995 (DOI: 10.1109/IEDM.1995.499187) on the inherent circuit speed limitations of interconnects, showing proportionality to the resistance (R) of the metal lines multiplied by the capacitance (C) of the dielectric insulation around the metal (Fig.1). The RC product thus should be minimized for maximum circuit speed, but the materials used for both the metal and the dielectric insulation around metal lines are at limits of affordability in manufacturing.



There are no materials that super-conduct electricity at room temperature, and only expensive and room-sized supercomputers and telecommunications base-stations can afford to use the

liquid-nitrogen cooling that is needed for known superconductors to function. Carbon Nano-Tubes (CNT) and 2D atomic-layers of carbon in the form of graphene can conduct ballistically, but integration costs and electrical contact resistances limit use. Copper metal remains as the best electrical conductor for on-chip interconnects, yet as horizontal lines and vertical vias continue to shrink in cross-sectional area the current density has reached the limit of reliability. The result is the increase in the number of metal layers to 13 for 14nm-node Intel microprocessors, while IBM used 15 layers for 22nm-node Power8 chips.

Low-k Dielectrics and Pore Sizes

[The dielectric constant](#) (“k”) of silicon oxide is ~ 4 , and ~ 3.5 with the addition of fluorine to the oxide (SiOF). Carbon-Doped Oxide (CDO or SiOC or SiOC:H) with $k \sim 3.0$ has been integrated well into interconnect stacks. Some polymers can provide k values in the 2.0-2.7, but they cannot be integrated into most interconnects due to lack of mechanical strength, chemical resistance, and overall stability. Air has $k=1$, and there have been specialized chips made using metal wires floating in air, but lack of physical structure results in poor manufacturing yield and weak reliability.

A clever compromise is to use both SiOC with $k \sim 3$ and air with $k \sim 1$ in a stack, which results in an integrated k value weighted by the percent of the volume taken up by each phase. Porous Low-k (PLK) with 10% porosity allows for an integrated k of ~ 2.7 for modest improvement, but increasing porosity to just 20% for $k \sim 2.4$ results in connected random pores that reduce reliability. To reliably integrate 20-30% air into SiOC, the pores cannot be random but must be engineered as discrete gaps in the structure.

In 2007, [IBM announced](#) that it would engineer air-gaps in microprocessors, but the company claimed to be using an extremely complex process for integration involving a self-assembled thin-film mask to anisotropically etch out holes between lines and then further isotropic etching to form elongated pores. Though relatively complex and expensive, this process allows for the use of any 2D layout for lines in a given metal layer.

Additive Air-gap Process-Design Integration

For fab lines that are still working with aluminum metal and additive dielectrics, air-gaps are a defect that occurs with imperfect dielectric fill. When not planned as part of the design, air-gaps formed in a lower-layer can be exposed to etchants during subsequent processing resulting in metal shorts or opens. However, **Figure 2** shows that it is possible to engineer air-gaps by Chemical-Vapor Deposition (CVD) of dielectric material into line-space structures with proper process control and design layout restrictions. Twenty years ago, this editor worked for an OEM on CVD processes for dielectric fill, and the process can be tuned to be highly repeatable and relatively low-cost if a critical masking step can be avoided. In 1998, Shieh et al. from Stanford (Shieh, Saraswat & McVittie. IEEE Electron Dev. Lett., January 1998) showed proof-of-concept for this approach to lower k values.

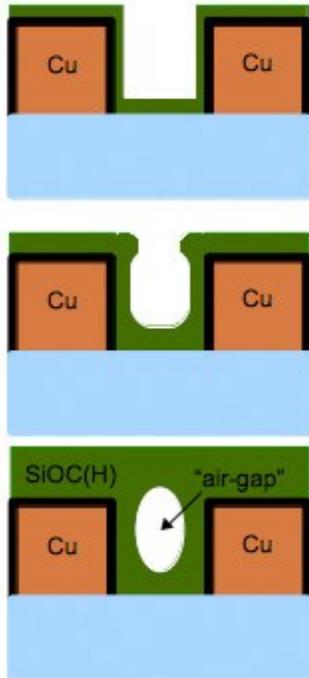


Figure 2: CVD can be easily tuned to initially coat sidewalls (top), then pinch-off (middle), and finally form a closed pore (bottom) during one step. (Source: Ed Korczynski)

Four years ago at IEDM 2010, Intel presented details of how to engineer air-gaps using CVD. [As this editor wrote](#) at that time in an extensive analysis:

The lithographic masking step is needed for two reliability reasons. First, by excluding air-gap formation in areas near next-layer vias, alignment between layers can be more easily done. Second, wide spaces are excluded where the final non-conformal CVD step wouldn't automatically pinch-off to close the gaps; leaving full SiOC(H) in wider spaces also helps with mechanical strength. The next layer is patterned with a conventional dual-damascene flow, with the option to add air-gaps.

Now we know that [Intel kept air-gaps](#) on the metaphorical shelf by skipping use at the 22nm-node. The 2014 IEDM paper from Intel will discuss details of 14nm-node air-gaps: two levels at 80nm and 160nm minimum pitches, yielding a 17% reduction in capacitance delays.

This process requires regularly spaced 1D line arrays as a design constraint, which may also be part of the reason for additional metal layers to allow for 2D connections through vias. Due to lithography resolution advantages with 1D “gridded” layouts, other logic fabs may soon run 1D

designs at which point additive air-gaps like that used by Intel will provide a relatively easy boost to IC speeds.